Research Article GU J Sci 37(1): 457-463 (2024) DOI: 10.35378/gujs.1218206

Gazi University

Journal of Science

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Voltage Dependent Profiles of the Surface States and Series Resistance (Rs) in the Al-(Cd:ZnO)-pSi Schottky Diodes (SDs) Utilizing Voltage-Current (IV) Characteristics

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Highlights

- This paper focuses on increasing the quality of metal-semiconductor-type Schottky diodes.
- Electrical parameters of Al-(Cd:ZnO)-pSi were investigated.
- This interlayer can be used instead of conventional insulator layers.

Article Info

Received: 12 Dec 2022
Accepted: 03 Mar 2023

Keywords

Comparative basic electrical parameters, I-V features and basic electrical parameters, The sources of interface traps

Abstract

In this work, the main electronic parameters of the performed Al-(CdxZn1-xO)-pSi Metal/Interface-layer/Semiconductor (MIS) type Schottky Diodes (SDs) were investigated by utilizing IV characteristics at 300 K. The $(Cd_xZn_{1-x}O)$ interfacial layer was grown on the pSi wafer by utilizing the sol-gel technique. Ideality-factor(n), potential barrier Φ_{Bo}, R_s, shunt resistance (R_{sh}), and rectification rate (RR) $(I_{forward}/I_{reverse})$ values were calculated based on thermionic emission (TE) theory and Cheung function between -4.5V and 4.5V. There parameters also varied for the samples with different doping ratios. Energy-dependent surface state profiles of them were also extracted from the forward bias IV data, and their magnitude was found on the order of $10^{12}eV^{-1}.cm^{-2}$ which is very appropriate for the MIS type SD. The values of n, barrier height (BH), Φ_{Bo}, and RR changed from 4.347, 0.582 eV, $5.74x10^3$ to 5.293, 0.607 eV, $2.83x10^6$. These results show that electronic parameters of these SDs are a strong function of voltage, calculation method, and the doping rate of the Cadminium (Cd) interfacial layer. The best ratio for Cd: ZnO was determined to be 30%; therefore, this interfacial layer may be used instead of traditional insulator layers to enhance the quality of Metal/Semiconductor (MS) type SDs.

1. INTRODUCTION

The electronic parameters and current-conduction-mechanisms (CCMs) of metal/interfacial-layer/semiconductor (MIS) type structures or Schottky diodes (SDs) are dependent on various factors such as the nature of BH, R_s, R_{sh}, interlayer, voltage, and temperature, as well as the calculation method [1]. Ordinarily, the semi-log IV curves diverge from ohmic behavior at sufficiently high current values. This deviation from ohmic/linear behavior is the result of Rs and interlayer. Because the voltage across the SD may be divided among them. In addition, when SD has barrier inhomogeneity, that is barrier has many patches or lower barriers that even the electrons with lower energy may pass over these lower-barriers or pinch-off and so this may cause an increase in the values of n, and a decrease in the apparent BH [2].

In recent years, transparent conducting-oxides (TCOs) have gained considerable interest, and become an important subject for researchers due to some important features such as huge conductivity, high charge density, electrochemical-stability, and transmittance [3]. Therefore, such materials can be used in different application areas, such as sensors, photo-transistors/diode/detectors, LEDs, and solar-cells [4]. The ZnO is

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used as potential TCOs in optoelectronics applications as an interlayer to insulate and react between metal and semiconductor, and it has a direct wide bandgap (≅3.37eV) and high binding energy (60meV) [5].

Although there are various methods for growing ZnO nanoparticles, such as MOCVD, MBE, magnetron sputtering (MS), spray/pyrolysis, and sol-gel spin coating (SGSC) method [6]. Among them, the SGSC is used more often due to its high homogeneity, ease of growth, lower cost, and temperature. The conduction of un-doped ZnO is not stable because of the changes in the properties of the surface, and so it can be doped with various-elements like CdO to improve its electrical features [6]. CdO has a lower bandgap energy (≅2.3eV) than ZnO [7].

In this study, a CdxZn1-xO interlayer with different contents of Cd (x= 0.1, 0.2, 0.3) was grown onto a pSi wafer by sol–gel technique to evaluate the effect of Cd incorporation in ZnO on the electronic characteristics. For this aim, the Al/ (Cd: ZnO)/pSi SD was fabricated on the same pSi substrate under the same conditions. After that, electronic features were calculated using the I-V data and compared for the different samples. All of the results indicated that the best SD has ratio of 30% Cd and 70% ZnO in terms of the low values of n, R_s, N_{ss}, and high rectification ratio ($RR=I_{forward}/I_{revese}$ at ±4.5V). Nevertheless, it needs to be noted that the sample with 20% Cd and 80% ZnO also shows similar features.

2. MATERIAL METHOD

($Cd_xZn_{1-x}O$) interlayer was grown on pSi semiconductor using sol-gel spin coating to fabricate the Al- (Cd: ZnO)-pSi SDs with various contents. The used p-Si wafer has <100> float-zone, 1" radius, 350 μm thickness, one-side polished, and $1.36\times10^{16}/cm^3$ density of acceptor atoms. After the cleaning process, the pSi substrate was dried with high-purity N_2, and high-purity Al was thermally grown on the whole back of the pSi substrate. In order to obtain ohmic contact with low resistivity and, the substrate was annealed at 450ºC in an N_2 chamber. Later, the prepared ($Cd_xZn_{1-x}O$) composites were grown onto the front of the pSi substrate via the sol-gel technique. In the last step, Al was also grown onto the ($Cd_xZn_{1-x}O$) thin film in the same evaporation system. Thus, the fabrication stage of Al-(Cd:ZnO)-pSi SDs was completed. More information on the structural analysis and the fabrication processes can be found elsewhere [2]. The IV characteristics of the samples were measured using a Keithley-2400 IV sourcemeter in the voltage range of (-4.5V) - (+4.5V) by 20 mV steps.

3. THE RESEARCH FINDINGS AND DISCUSSION

A typical semi-log. IV curves of the Al-(CdZnO)-pSi SD for the different doping ratio of Cd into ZnO are given in Figure 1. As is seen in the figure, lnI vs. V curves for each sample show good rectifying behavior and also have a good linear range in the wide voltage region at moderate bias voltages. However, at higher voltages, lnI vs. V plots diverge from ohmic behavior owing to the existence of R_s and interlayer. In addition, while the (0.2:0.8) and (0.3:0.7) contents show good saturation in the negative voltage regime, (0.1:0.9) content does not show a saturation behavior in this range owing to the image force lowering of BH, the generation recombination current (I_{GR}) and the interlayer.

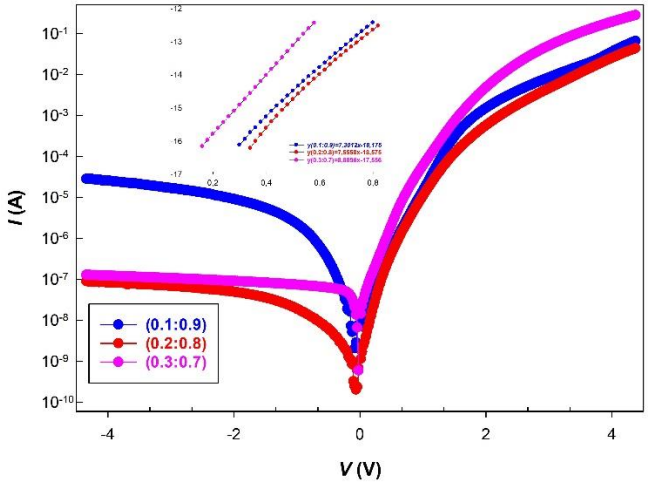

Figure 1. *The semi-log. IV curves of the Al/CdZnO/pSi structures*

When the MS or MIS structure has R_s, and n is higher than 1, the relation between current and voltage in the positive voltages (V≥3(kT/q) in terms of TE over the barrier is given as follows [1,8]:

$$I = SA^{*}T^{2}\, exp\left(-\frac{q}{kT}\Phi_{B0}\right)\left[exp\left(\frac{q(V-IR_S)}{nkT}\right)-1\right]. \quad (1)$$

Here, S, A^{*}, T, and R_s are the diode area, the Richardson constant (≅32A/cm^{2}K^2 for pSi), the temperature in Kelvin, and series resistance of the structure, respectively. The term V-IR$_s$ is the voltage drop, V_d, on the diode. Expression in front of square-brackets is known as the reverse current (I_o or I_s), which may be found by fitting the linear regime to the voltage axis of the semi-log. IV curve at V=0. Thus, Equation (1) can be rearranged as follows:

$$Ln(I) = Ln(I_S) + \left(\frac{qV_d}{kT}\right) \quad . \quad (2a)$$

Thus, the value of n can be estimated in the semi-log IV curve as;

$$n = \frac{q}{kT}\left(\frac{dV_d}{d(lnI)}\right) = 1 + \frac{\delta_i}{\varepsilon_i}\left(\frac{\varepsilon_s}{W_D} + qN_{ss}\right). \quad (2b)$$

The Φ_{Bo} value was calculated using I_s, and rectifier contact-area (S) as given follows:

$$\Phi_{B0} = \frac{kT}{q} Ln\left(\frac{T^2A^{*}S}{I_0}\right). \quad (2c)$$

The electronic parameters of the SDs are tabulated in Table 1. The values of R_s, R_{sh} of these structures were also extracted using Ohm's law [$R_i = (dV_i/dI_i)$] and lnR_i vs. V_i curves of these diodes were given Figure 2. It is seen that the diode resistance (R_i) depends on voltage (Vi), such that resistance values at high forward & reverse voltages correspond to R_s and R_{sh}, respectively.

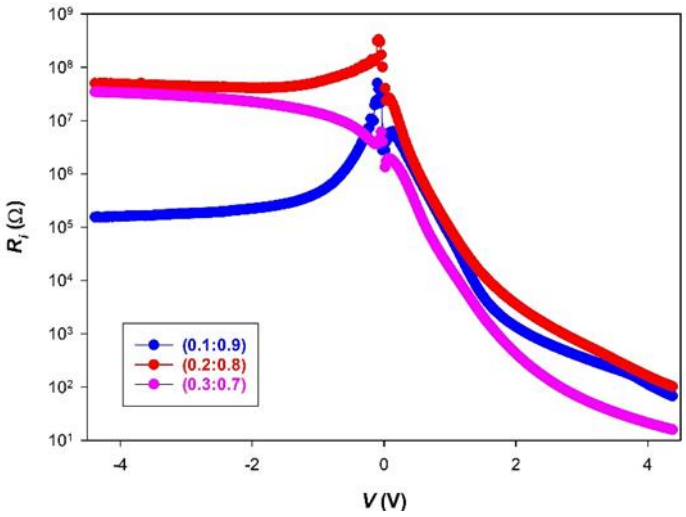

Figure 2. *The lnR_i vs. V_i plots of the Al- (Cd: ZnO)-pSi structures*

Table 1. *The calculated some electronic parameters of the Al-(CdZnO)-pSi structures*

Cd: ZnO (%)	I_s (A)	n	Φ_{Bo} (eV)	R_s (at 4.5V) (Ω)	R_{sh} (-4.5V) (MΩ)	RR (±4.5V)
(0.1:0.9)	$1.28x10^{-8}$	5.293	0.597	34.12	0.20	$5.74x10^3$
(0.2:0.8)	$8.57x10^{-9}$	5.115	0.607	51.71	31.30	$6.06x10^5$
(0.3:0.7)	$2.37x10^{-8}$	4.347	0.582	10.69	30.20	$2.83x10^6$

As is seen in Table 1, the minimum/maximum values of the I_s, n, Φ_{Bo}, R_s, R_{sh}, and RR changed between $8.57x10^{-9}$- $2.37x10^{-8}$ A, 4.347- 5.293, 10.69 – 51.71 Ω, 0.20 – 31.30 MΩ, and $5.74x10^3$- 56.06, respectively. These values suggest that the best sample has Cd ratio of 30% because it has lower R_s, n, Is and higher R_{sh}, RR, and BH. The basic electrical parameters (n, Φ_{Bo}, R_s) were also extracted using the Cheung functions given below [9]

$$\frac{dV}{d(lnI)} = IR_s + \left(\frac{nkT}{q}\right). \tag{3a}$$

The n, R_s, and Φ_B values of these SDs can be extracted using Equations (3a) and (b) and the related plots are given in Figures 3(a-c) for each SD. As can be seen from Figures 3(a-c), both the *dV/d)lnI) vs I and H(I) vs I* have good linear behavior over wide range current in the forward bias region, As can be seen from these figures, the slope of these two plots in these figures, directly gives the value of R_S, but n and Φ_B values of these SDS were calculated from the intercept of these plots by using Equations 3(a) and (b), respectively. The observed some little discrepancies in the n, R_s, and Φ_B values obtained these Cheung function are the result the nature of these calculation methods which are corresponding different forward bias voltages and voltage dependent of them

$$H(I) = V - \frac{nkT}{q}\ln\left(\frac{I}{AA^*T^2}\right) = IR_s + n\Phi_B. \tag{3b}$$

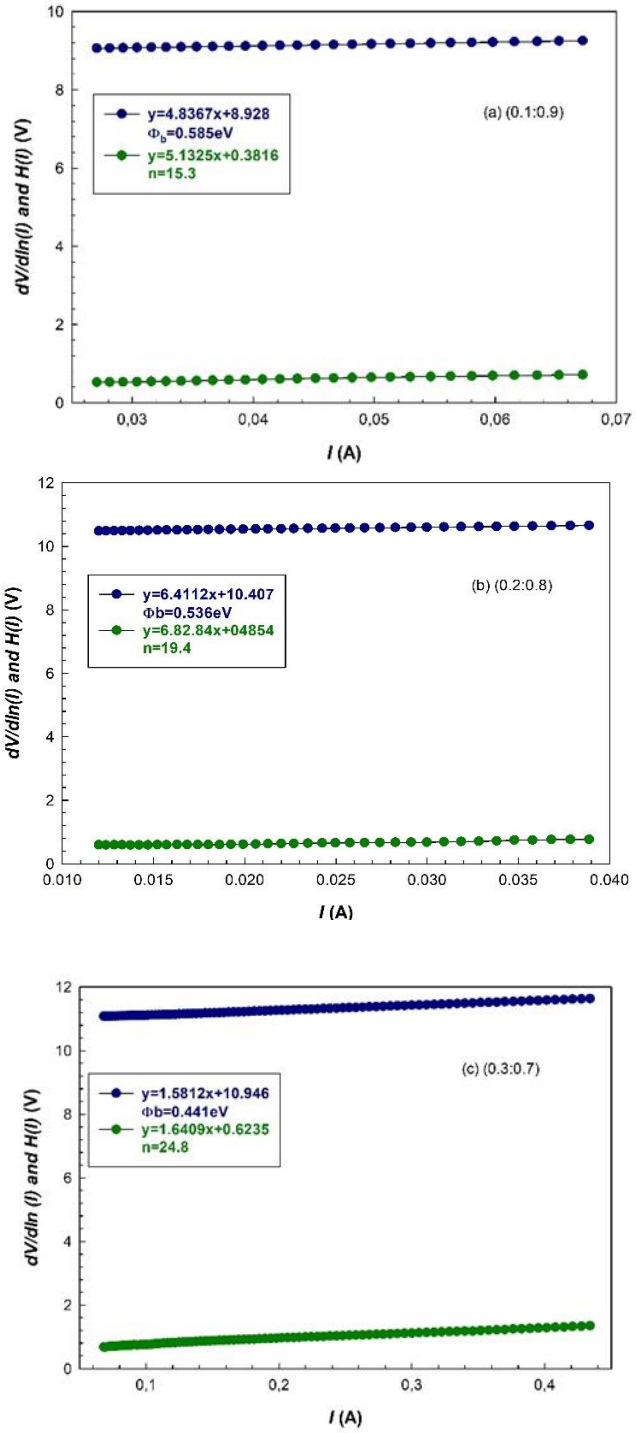

Figure 3(a-c). *The first and second Cheungs curves of the Al- (Cd: ZnO)-pSi structures*

The presence of surface states (N_{ss}) localized at the M/S interface in the forbidden bandgap is also effective on the performance of MS/MIS SDs. According to Card and Rhoderick [3,10], the value of N_{ss} may be evaluated as a function of energy using the forward bias *I-V* data by considering n(V) and Φ_b(V). Thus, the values of N_{ss} and (E_{ss}-E_v) were calculated using Equations 4(a) and (c) [11]

$$\Phi_e = \Phi_{B0} + \beta(\mathrm{V} - \mathrm{I}R_s) = \Phi_{B0} + \left(1 - \frac{1}{n(V)}\right)(V - IR_s) \quad (4a)$$

$$E_{ss} - E_v = q(\Phi_e - V). \quad (4b)$$

In Equation (4a), $\beta = d\Phi_e/dV$ $(= 1 - 1/n(V))$ is the voltage coefficient of BH. Thus, the plot of N_{ss} vs. (E_{ss}-E_v) can be drawn using Equations (2b), (4a), and (4b) [3,10]:

$$N_{ss}(V) = \frac{1}{q}\left(\frac{\varepsilon_i}{\delta}\,(n(V) - 1) - \frac{\varepsilon_s}{W_D}\right) \quad (4c)$$

where δ is the thickness of the interlayer and W_D is the width of the depletion regime considered. Moreover, ε_i and ε_s are the interlayer and semiconductor permittivity, respectively [12]. In this way; N_{ss} - (E_{ss}-E_v) profiles for three Schottky diodes were obtained by using Equations (4b) and (c) and given in Figure 4. It is quite clear that the N_{ss} values for three samples increase from midgap energy towards the top of valance band edge (*Ev*) and changed between the orders of 10^{11} $eV^{-1}cm^{-2}$ and 10^{12} $eV^{-1}cm^{-2}$. The mean values of N_{ss} for the sample with Cd:ZnO (0.3:0.7) are lower than the others due to the passivation effect of the interfacial layer [1,13,14].

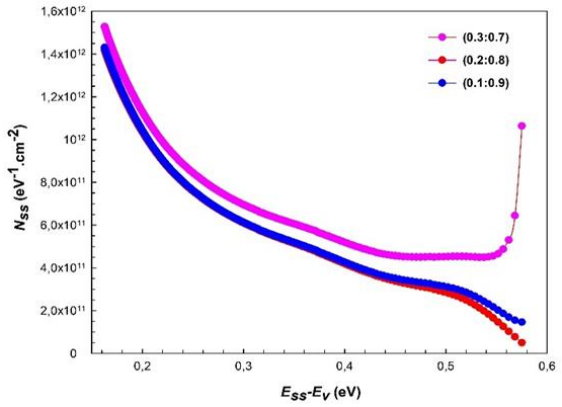

Figure 4. *N_{ss}-(E_{ss}-E_v) plots of the Al-(CdZnO)-pSi structures*

4. RESULTS

In this work, ($Cd_xZn_{1-x}O$) with varying x (0.1, 0.2, and 0.3) was grown on the pSi substrate utilizing the sol–gel technique to assess the impact of Cd inclusion in ZnO on the electrical characteristics of Al- (Cd: ZnO)-pSi SDs at room temperature. Therefore, three Al/(Cd:ZnO)/pSi structures with different Cd ratios were fabricated using the same pSi substrate to compare their basic electronic parameters (*Is*, *n*, Φ_{Bo}, R_s, R_{sh}, *RR*, and N_{ss}) obtained from the IV characteristics. The minimum and maximum values obtained for these parameters are $8.57x10^{-9}$- $2.37x10^{-8}$A, 4.347 - 5.293, 10.69 – 51.71 Ω, 0.20 – 31.30 MΩ, and $5.74x10^3$ - 56.06, respectively. The N_{ss} vs. (*Ess-Ev*) profiles of these diodes were also determined using the forward bias *I-V* data considering ideality factor and barrier height are voltage dependent. The values of N_{ss} for these three samples increased from the midgap energy towards the top of the valance band edge (Ev) and changed between the orders of 10^{11} $eV^{-1}cm^{-2}$ and 10^{12} $eV^{-1}cm^{-2}$ and also N_{ss} of Al/($Cd_{0.3}Zn_{0.7}O$)/pSi is lower than those of the other samples due to the passivation-effect of the interlayer. In conclusion, the electrical parameters of the investigated SDs indicate that the best Cd ratio is 30 %.

ACKNOWLEDGEMENT

Some parts of this study are presented at the 9th International-Conference on Materials-Science and Nanotechnology for Next-Generation (MSNG-2022).

CONFLICTS OF INTEREST

No conflict of interest was declared by the authors.

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