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Research Article

An Electronically Tunable Low Power Low Pass Filter Employing Capacitor Multiplier for Biomedical Applications

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Abstract

In this work, a novel 0.9nW low pass filter is proposed using 0.18µm TSMC technology in Cadence environment to reject unwanted signals of biomedical applications. Active RC filter is designed with a new capacitor multiplier implementation providing high multiplication factor along with low power consumption. The designed circuit operates with ±0.3V supply voltages with DTMOS technique. At the same time, the power consumption of the proposed circuit is very low that can be implemented in implantable devices. The bandwidth of the designed filter is adjustable between 500mHz and 65Hz. In terms of Figure of Merit, the proposed filter outperforms the recommended circuits in the literature.

Keywords: Biomedical Applications, Low Pass Filter, Operational Transconductance Amplifier (OTA), Dynamic Threshold MOS (DTMOS)

Biyomedikal Uygulamalar için Kapasite Çarpıcı Kullanan Elektronik Olarak Ayarlanabilen Düşük Güçlü Alçak Geçiren Süzgeç

Öz

Bu çalışmada, biyomedikal uygulamaların istenmeyen işaretleri süzmek için Cadence ortamında 0.18µm TSMC teknolojisi kullanılarak yeni bir 0.9nW düşük geçiş filtresi önerilmiştir. Aktif RC filtresi, düşük güç tüketimi ile birlikte yüksek çarpma faktörü sağlayan ve üç katmalı OTA yapısından oluşan yeni bir kapasite çarpıcı devresi ile tasarlanmıştır. Tasarlanan filtrenin bant genişliği 500mHz ile 65Hz arasında ayarlanabilmektedir. Aynı zamanda önerilen devrenin güç tüketimi taşınabilir cihazlarda uygulanabilecek kadar düşüktür. Önerilen kapasite çarpıcı devresi özellikle güç tüketimi ve çalışma gerilimi açısından literatürde önerilen devrelerden daha yüksek performans göstermektedir.

Anahtar Kelimeler: Biyomedikal Uygulamalar, Alçak Geçiren Süzgeç, OTA, DTMOS

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1. Introduction

Today, the demand for wireless devices such as portable biomedical devices, smartphones, laptops, tablet computers, and various wireless devices is constantly increasing. Integration of system plays a role as important as power dissipation for portable devices. Industry 4.0 applications will further expand the use of mobile devices [1]. The portability of digital circuits is increased by the CMOS technology produced in small dimensions. However, the fact that CMOS transistors produced in small sizes cannot be used effectively in analog circuit design has led to the search for new methods to design analog circuits [1,2].

CMOS technology is ideal in terms of the circuit, which needs to be designed with low power consumption. The minimized supply voltage is functional to reduce the power consumption of the circuits. The threshold voltage cannot be downscaled by the same extent as the supply voltage in modern small size CMOS technologies gets smaller. The high V_{TH} is required to obtain a low current when the transistor is switched off. The current injection of MOSFETs is generally in several nano amper ranges in the weak inversion region that will be functional due to a minimized supply voltage [3,4]. Also, the circuit topology must be suitable for the minimized supply voltage. The above requirements encourage the innovative design strategies in CMOS analog circuit design [5-8]. For example, the Dynamic Threshold MOS (DTMOS) technique is an example of new design strategies proposed for CMOS technology [9,10]. Particularly, low power consumption has increased the importance for the circuits used in the Internet of Things applications that are becoming widespread in our lives [11,12].

In biomedical signal acquisition systems, low frequency filters are used to reject unwanted signals and extract low frequency bio-potential signals. The rejection of out-of-band noise and interference suppression is realized by using these low frequency filters [13,14]. Bio-potential signals are weak analog signals. The amplitude of bio-potential signals extends between 1μV to 10mV while the frequency of bio-potential signals ranges from less than 1Hz to 10kHz [15]. In the integration of low pass filters operated at low frequencies, the filter topology of RLC and RC are not practical due to the high costs [16]. Switched capacitor filters are not preferred to collect bio-potential signals because they are affected by leakage currents in the switching [17]. In biomedical systems, to catch the low frequency operation, G_m - C filters are widely used [18]. In G_m –C filters, the cut-off frequency is determined by the G_m / C ratio, where G_m is defined as the transconductance of the operational trans-conductance amplifier (OTA) and C is integrated capacitor. To implement the filter at low cut-off frequencies, large valued C and pretty small G_m are preferred. In this respect, various design techniques have been proposed in the literature to obtain low G_m to OTAs [19,20].

However, capacitance multiplier circuits are commonly used for applications described in the literature as sub-hertz [21-23]. In an RC network, circuits operating at low frequencies are designed by increasing the time constant with a huge value of resistance or capacitance. To improve the time constant of RC network, the multiplied capacitance can be implemented instead of conventional capacitor.

In this study, a low pass filter is designed to meet the wireless features of biomedical applications, with a wide range of settings based on capacitor multiplier. The design consumes very low power, suitable for bio-potential signal acquisition systems used in the applications of Internet of Things. The presented circuit is implemented with DTMOS transistors in sub-threshold region. Meanwhile, supply voltages of the design are ±0.3V. Overall simulations are realized in Cadence environment. Also, the performance of the circuit is verified using 0.18μm TSMC technology.

This paper is organized as follows. In the second section, circuit design of the capacitance multiplier is given. In the third section, the CMOS realization of capacitor multiplier is given

while second order Butterworth filter structure and its layout are given in forth section. Transient and AC analysis of the designed filter are given in forth section with noise analysis. Additionally, the performance of the designed filter is justified by comparing conventional designs in terms of Figure of Merit. Section V gives some conclusions.

2. Circuit Design of Proposed Capacitance Multiplier

One of the most limiting problems in the design of integrated circuits is the large area occupation on the integration of passive circuit elements such as resistance, inductance and capacitance. Continuous time applications in which the use of component (R, L and C) multipliers is inevitable have to deal with the problem of integration of high-value passive circuit elements. There is widespread research in the literature on this critical issue. In this respect, the design of capacitance multiplier circuits is of greater importance than others. Although it is used in RF designs with the general acceptance of inductance, capacitor is an indispensable circuit element in most of circuits such as capacitive low frequency filters, analog to digital converters, and digital to analog converter. In particular, $G_m - C$ filters including multiplier structures have been widely used in the literature. Such capacitance multiplier circuits have attractive properties of temperature insensitive C-values with good stability [24–27].

The categorization of capacitor multipliers designed in the literature can be divided to two parts as voltage and current-mode. The voltage-mode capacitor multiplier circuits are generally used for frequency compensation. In this regard, capacitor multipliers designed with operational amplifiers can be given as an example of voltage mode multipliers. The current mode multipliers can be designed with CCII, OTA and etc. The second generation current conveyor (CCII) has also been used to realize C-multiplier circuits due to its attractive characteristics [22,28]. Even though CCII are suitable for the multiplier design with high multiplication factor, OTAs are more attractive building blocks for the reconfigurable design of multiplication factor. A large number of OTA-based C-multiplier circuits using bias adjustment have been reported in literature [27,29].

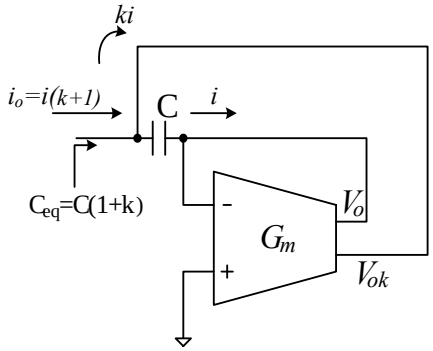


Figure 1. OTA based capacitor multiplier.

The simplest OTA based capacitor multiplier reported as current mode is shown in Figure1, while the proposed circuit is given in Figure 2. The first and second OTAs used in the implementation of the multiplier have multiple current outputs. In this topology, "i" on C is sensed with the low value of G_{m1}. Multiplication of the sensed current by multiplication factor denoted as k, is obtained with higher gain of $G_{m1}.G_{m2}.G_{m3}.R_{o1}.R_{o2}$ where R_o denotes the output impedances of the each OTA. In this respect, i_o is equal to "i" times $(1+k)$, while C_{eq} is equal to the $C.(1+k)$. As a result, output current shown as i_o in the Figure 2, gives k times higher value of the current in (1) approximately. It should be noted that this simple scheme based on traditional topology provides good accuracy in spite of limited multiplication factor

and allows only single-ended applications, whereas the current multiplication inside single OTA with current mirror or other methods increases the consumption of power and the occupation area on the silicon [30].

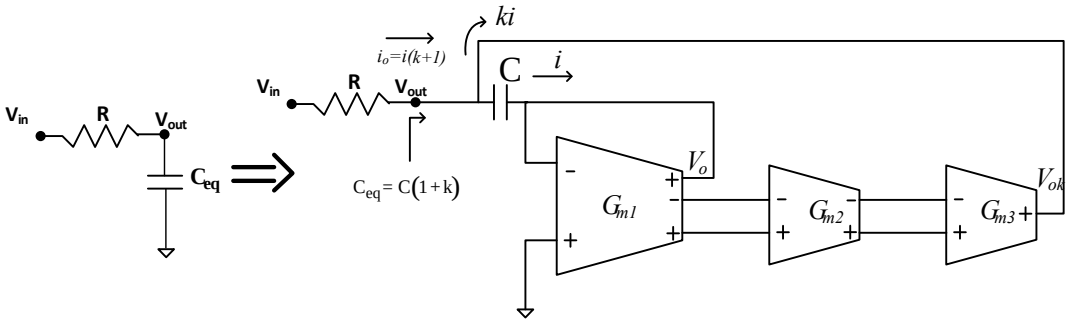


Figure 2. Proposed filter with capacitor multiplier.

This proposed topology is developed version of OTA based multipliers reported in literature [27], [31]. In this topology, the multiplied current $k.i$ is obtained with three cascaded OTA. The non-inverting output of the first cell gives V_o, while V_{ok} is the non-inverting output of third cell. The third OTA is driven with the fully differential output of second OTA, while the fully differential output of first OTA drives the second OTA. The multiplication factor of k is maximized by selecting the conductivity of the second and third cell as high as possible. The equation of i is given in (1). G_m defines the transconductance of OTA, where V_P is non-inverting input of OTA and V_N is inverting input of OTA as well.

$$i = G_{m1}(V_P - V_N) \tag{1}$$

In this respect, taking into consideration output impedances of the OTAs, impedance seen from V_{out} node can be given in the following form:

$$Z = \frac{sC + G_{m1}}{sC(G_{m1} + 4R_{o1}R_{o2}G_{m1}G_{m2}G_{m3})} //R_{o3} \tag{2}$$

In the subthreshold operation, very high output impedances of OTAs can be obtained. Hence, for the simplicity of calculations, third OTA's output impedance can be ignored. Furthermore, in the low operating currents with the help of DTMOS technique, G_{m1} can be easily tuned from a few nS up to a couple of 10 nS. For the base capacitance (C) values in the range of a couple of 10pFs, (2) can be easily simplified as follows for the biomedical applications with the operating frequency up to around 100Hz:

$$Z \cong \frac{G_{m1}}{sC(G_{m1} + 4R_{o1}R_{o2}G_{m1}G_{m2}G_{m3})} \tag{3}$$

Moreover, if G_{m1} is increased up to 10nS, (3) keeps capacitance multiplier behavior up to 10kHz approximately. In this point of view, "k" multiplication factor can be approximated as follows:

$$k \cong 4R_{o1}R_{o2}G_{m2}G_{m3} \tag{4}$$

$$\omega_{cut-off} \cong \frac{1}{kRC} \tag{5}$$

In this view, (4) brings a large amount of capacitance value at the V_{out} node to attain very low operating frequency region in the biomedical applications. According to (4) and (5), cut-off frequency of the proposed first order low pass filter can be safely adjusted by output impedances and transconductance values of the three cascaded OTA stages. Hence, bias currents of the OTAs play an important role in determining the cut-off frequency of the proposed filter with capacitance multiplier. In the next sections, DTMOS technique is given with the CMOS implementation of the OTAs, whereas the operating mechanism of the filter is justified with the post layout simulations with regard to different bias currents of each OTAs.

3. CMOS Implementation of Low Pass Filter

Biomedical applications such as implantable and portable devices must be provided with low power operation. MOS transistors operating in deep sub-threshold region consume very low power. Generally, the designed circuits in sub-threshold region designed with MOS transistors have low supply voltage. For example, when the supply voltage of designed circuit with saturated MOS transistors for the 0.18µm technology is 1.8V, the supply voltage of this circuit with MOS transistors in weak inversion region for the 0.18µm technology can be lower than 0.7V.

Moreover, to improve the performance of the MOS transistors with the same power dissipation, different techniques such as Dynamic Threshold Metal Oxide Semiconductor (DTMOS) are investigated in literature [9], [32]–[36]. DTMOS can support high current gain and with low threshold characteristics and its leakage current is minimized. Because of its ultra-low voltage capability, DTMOS is very practical to design ultra-low voltage analog circuits [37], [38]. The idea of DTMOS is established by connecting the transistor gate and body to each other. This connection changes the threshold voltage. The threshold voltage of DTMOS is given in (6). The proposed CMOS circuit is implemented with DTMOS transistors as given in Figure 4, whereas DTMOS realization symbol is illustrated in Figure 3.

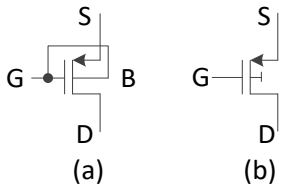


Figure 3. (a) The realization of DTMOS with standard MOS (b) The representation of DTMOS

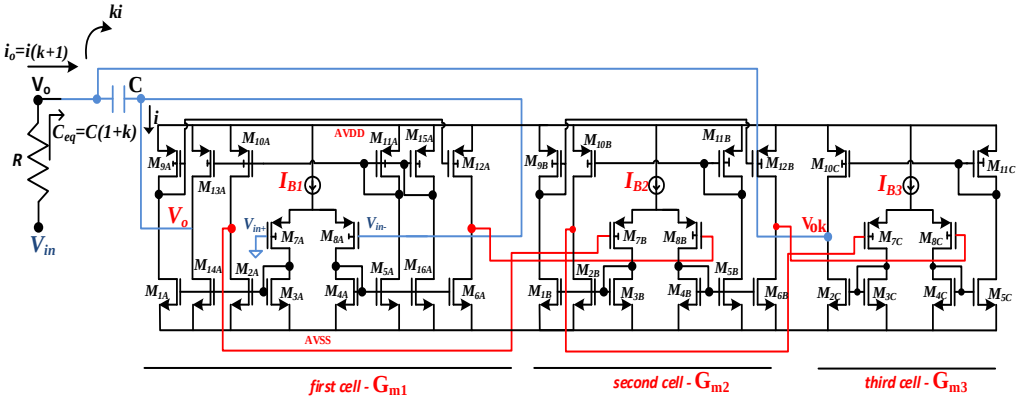


Figure 4. CMOS implementation of proposed filter.

$$|V_{th,p}| = |V_{th0,p}| + \gamma_p \left(\sqrt{|2\Phi_F| + V_{SB}} - \sqrt{|2\Phi_F|}\right) \tag{6}$$

The implementation of the proposed circuit is suitable to obtain high multiplication factor. The implementation of designed structure is advanced version of recently recommended cell-based variable transconductance amplifier [39], [40]. Three cascaded symmetric OTAs compose the structure. The first OTA is called "first cell" while the second OTA is "second cell" and the third one is "third cell". Table 1 gives the size of the transistors. In the proposed structure, the fully differential output is easily implemented by symmetrical OTA to drive the second and the third cells. In this respect, (7) gives the gain of each OTA in the sub-threshold region.

Table 1. The size of transistors.

Transistors	*First Cell* *W/L*	*Transistors*	*Second Cell* *W/L*	*Transistors*	*Third Cell* *W/L*
M_{1A}, M_{2A}, M_{5A}, M_{6A},	2µm/360nm	M_{1B}, M_{2B}, M_{5B}, M_{6B},	6µm/360nm	M_{2C}, M_{5C}	6µm/360nm
M_{9A}, M_{10A}, M_{11A}, M_{12A}	2µm/360nm	M_{9B}, M_{10B}, M_{11B}, M_{12B}	6µm/360nm	M_{10C}, M_{11C}	6µm/360nm
M_{7A}, M_{8A}	360nm/360nm	M_{7B}, M_{8B}	5µm/360nm	M_{7C}, M_{8C}	5µm/360nm
M_{3A}, M_{4A}	4µm/220nm	M_{3B}, M_{4B}	2µm/220nm	M_{3C}, M_{4C}	2µm/220nm
M_{13A}, M_{14A}, M_{15A}, M_{16A}	2µm/360nm	-	-	-	-

$$K_{VO} = \frac{g_{m8} \cdot \frac{\left[\frac{W}{L}\right]_5}{\left[\frac{W}{L}\right]_4}}{g_{ds5} + g_{ds11}} \tag{7}$$

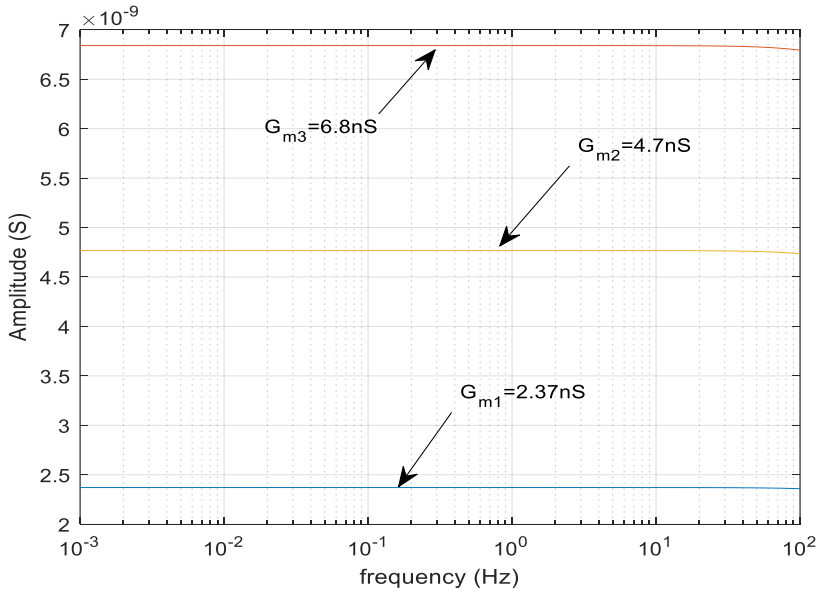
g_m and r_o of MOS transistor are shown in (8) for the sub-threshold region. g_m defines the transconductance of transistor, while r_o is the output impedance of transistor. κ denotes the subthreshold gate efficiency, whereas λ is the parameter of channel length modulation. $V_T = k.T\ /\ q$ is the thermal voltage (k - Boltzmann constant, T - absolute temperature, q - elementary charge).

$$g_m \cong \frac{\kappa . q . I_D}{kT}, \quad r_o = \frac{1}{\lambda I_D} \tag{8}$$

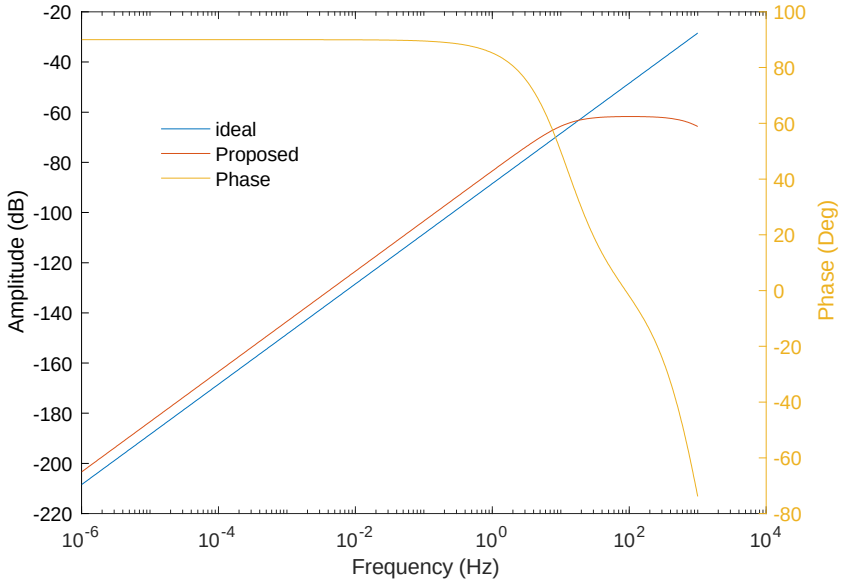
In the proposed circuit, V_o is obtained from the first cell with the transistors of M_{13A}, M_{14A}, M_{15A}, M_{16A}, M_{2A}, M_{5A}, M_{10A}, M_{11A}, whereas V_{ok} comes from the third cell to increase the multiplication factor by passing through the first and second cells. The gain of $(k+1)$ is maximized to be as large as possible by this way. (6), (7) and (8) are used to determine the dimensions of the transistors in Figure 4.

4. Layout and Post-Layout Simulations

Minimum power consumption of the designed circuit is 0.98nW under the minimum biasing current. The simulated results for the transconductance of the cells in the proposed topology are illustrated in Figure 5 (a). In this respect, transconductance of the first cell can be observed around 2.37nS for I_{B1}=0.1nA current. Also, transconductance of the second cell is given as 4.7nS for I_{B2} = 0.1nA, while transconductance of the third cell is found as 6.8nS for I_{B3} =0.1nA. Furthermore, multiplication factor for 10pF base capacitance is simulated as shown in Figure 5 (b). Multiplied capacitance is around 60nF, while the multiplication factor is 6000 with 90^0 phase response. According to Figure 5 (a) and (b), there is a good agreement between simulation results and equations of (2), (3), and (4) presented in the previous section.



(a)



(b)

Figure 5. (a) Transconductance of first, second and third cell, (b) multiplication factor for 10pF base capacitance.

Figure 6 gives the layout of the designed filter. The occupied area on chip without electrostatic discharge (ESD) protection of the designed circuit is 71.99µmx115.05µm; 0.0083mm^2. The post-layout simulation of the second-order low pass filter is shown in Figure 7. The cut-off frequency of the designed filter is 500mHz for 100kΩ resistance with 10pF base capacitance.

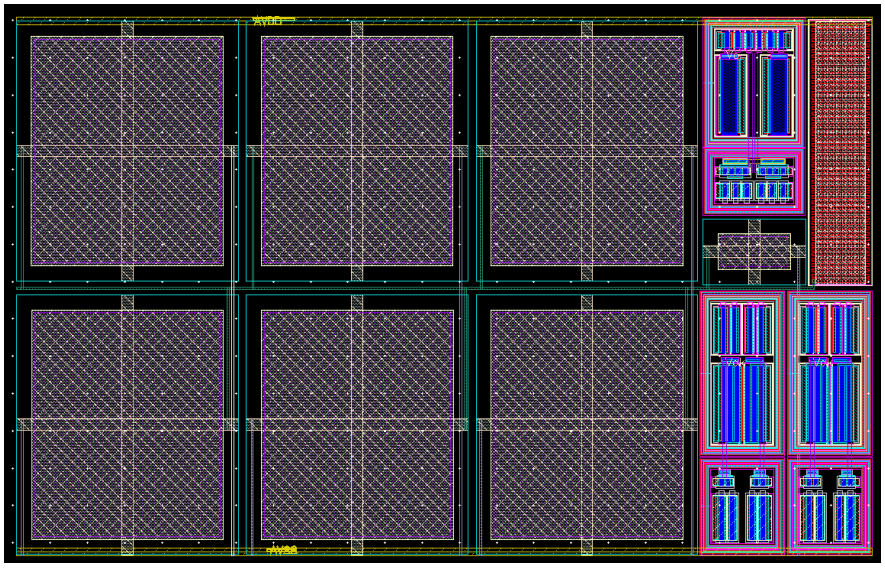


Figure 6. Layout of the proposed circuit (occupies 0.0083mm^2 area).

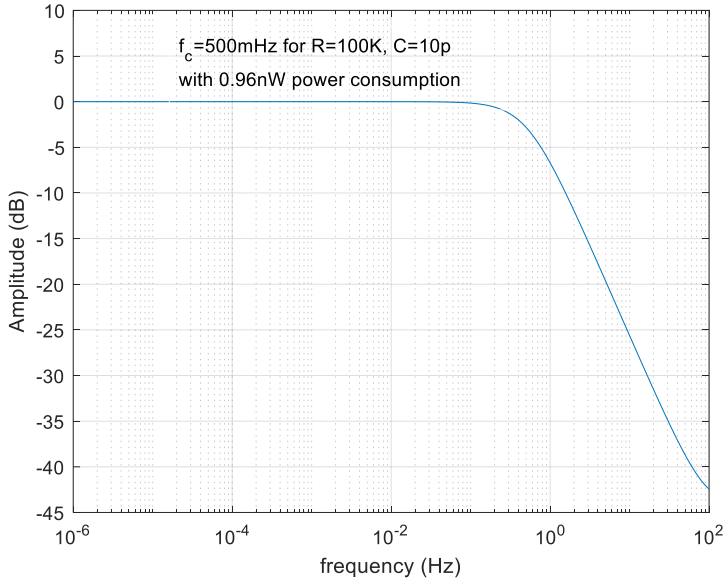


Figure 7. Post-layout simulation of designed filter for R=100kΩ and C=10pF (base capacitor).

THD performance of the filter for peak-to-peak input signal at 1mHz frequency is given in Figure 8. The total harmonic distortion is 0.12% for 100mV peak-to-peak input signal at 1mHz, while output signal of the proposed filter is given in Figure 9 for the same input voltage signal. Furthermore, input referred noise is 9.09µV/sqrt(Hz) as given in Figure 10. Spurious Free Dynamic Range (SFDR) of the designed filter is around -78.2dBc. The analysis of SFDR is given in Figure 11 at 1mHz input frequency for 100mV peak to peak input signal.

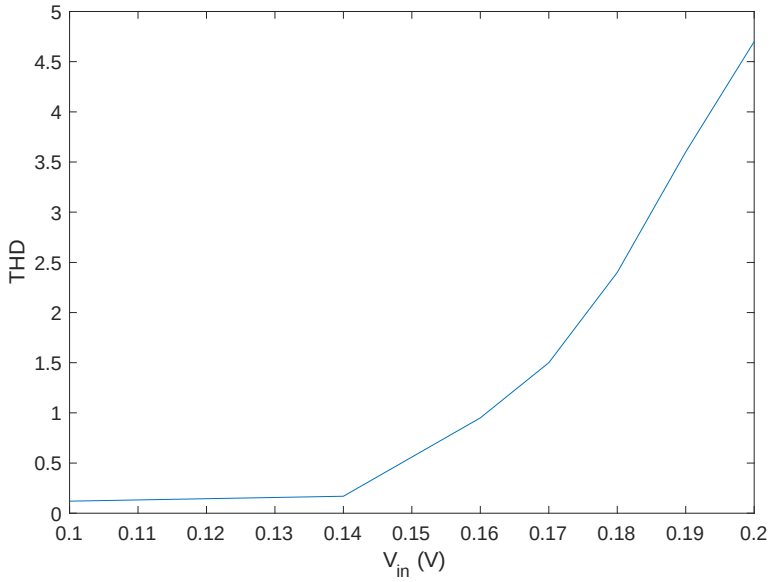


Figure 8. Linearity check of the designed filter (THD = 0.12% for 100mV of peak input signal at 1mHz).

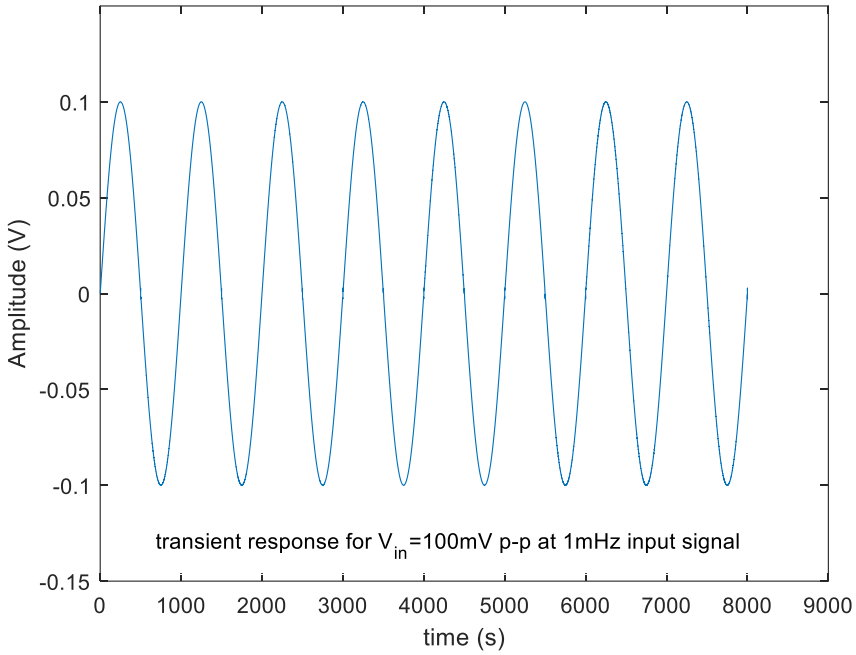


Figure 9. Transient response of the designed filter (THD = 0.12%).

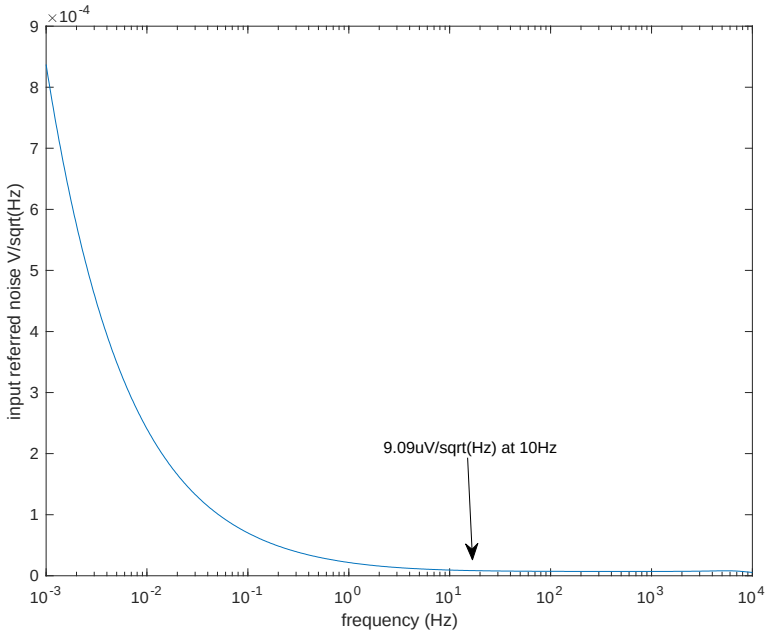


Figure 10. Input referred noise of the designed filter.

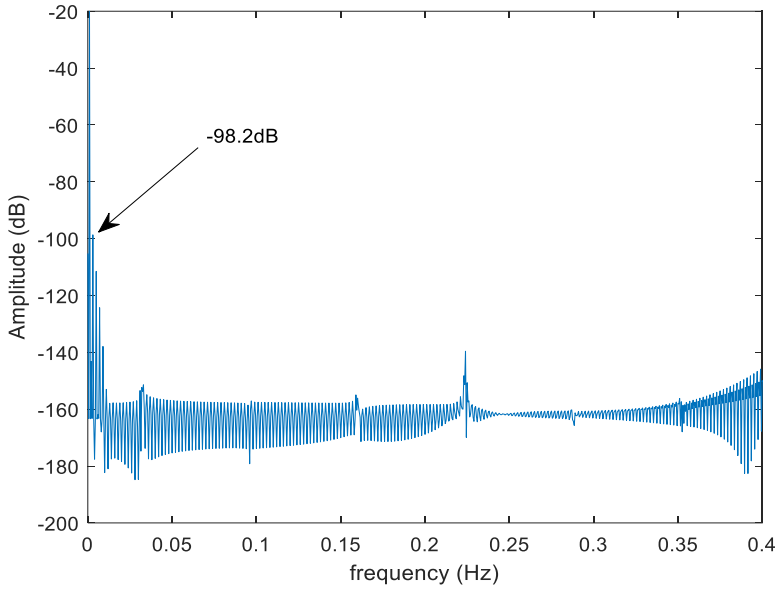


Figure 11. Spurious Free Dynamic Range.

The cut-off frequency of the designed filter can be adjustable with the biasing current as given in Figure 12. Table 2 gives the biasing current of each cell versus f(-3dB) as well. The configurability of the designed filter can be realized by changing G_{m2} and G_{m3} with different I_{B2} and I_{B3}, respectively. Also, output impedances of the first and second OTAs in the proposed filter structure in Figure 2 play an important role for the cut-off frequency. In this point of view, Figure 12 and Table 2 are in good agreement with equations of (3), (4), (5), (7) and (8) presented in the previous sections. Corner analysis of the designed filter including variations of process (ss, tt, ff, sf, fs), temperature (-40^{o}C, 85^{o}C), and power supplies of AVDD and AVSS (0.33V, 0.27, -0.33V and -0.27V) is realized to check resilience of the performance. It can be said that the filter performance remains in acceptable limits. The low pass function of the designed filter is preserved under the worst cases. In addition, Figure 13 gives the Monte Carlo analysis. To investigate resilience of proposed filter, cut-off frequency of the filter is analyzed under the Monte-Carlo seeds. The Monte-Carlo simulation runs including distinct process corners (ss, sf, fs, ff) also transistor mismatches by changing transistors' channel lengths and/or width independently. In the end of this process, it should be noted that standard deviation of the cut-off frequency is lower than 10%, where cut-off frequency of the designed filter is around 24Hz while standard deviation is 1.47Hz. In the Monte Carlo analysis, all process variations and mismatches are taken into consideration for 100 independent runs. Standard deviation of the designed filter for 1.47Hz while cut-off frequency is 24Hz. Table 3 gives the detailed comparison of the proposed circuit with other studies in the literature. The design is considered to give promising results when compared to the defined Figure of Merit given in (9).

$$FoM = \frac{power}{dynamic\ range\ x\ order} \tag{9}$$

Table 2. Biasing current versus f_{-3dB}

I_{B1}	I_{B2}	I_{B3}	f_{-3dB}
0.1nA	0.1nA	0.1nA	***500mHz***
0.1nA	0.1nA	1nA	***3Hz***
0.1nA	1nA	0.1nA	***9Hz***
1nA	1nA	1nA	***24Hz***
1nA	1nA	10nA	***65Hz***

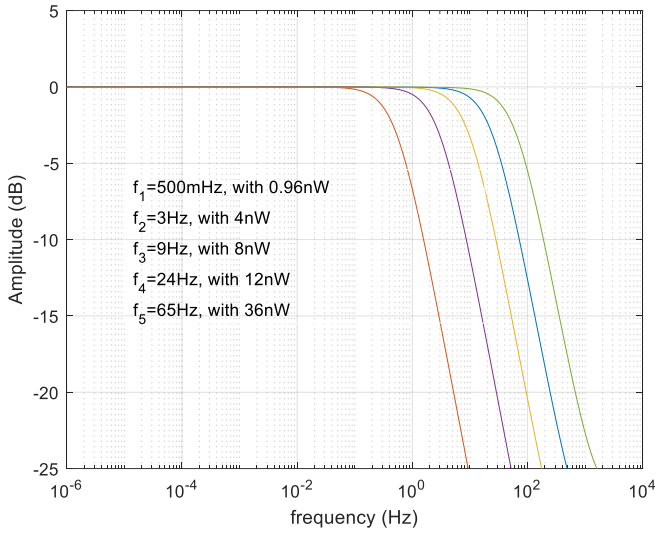


Figure 12. The reconfigurable output of the designed filter for different bias currents of three cascaded cells.

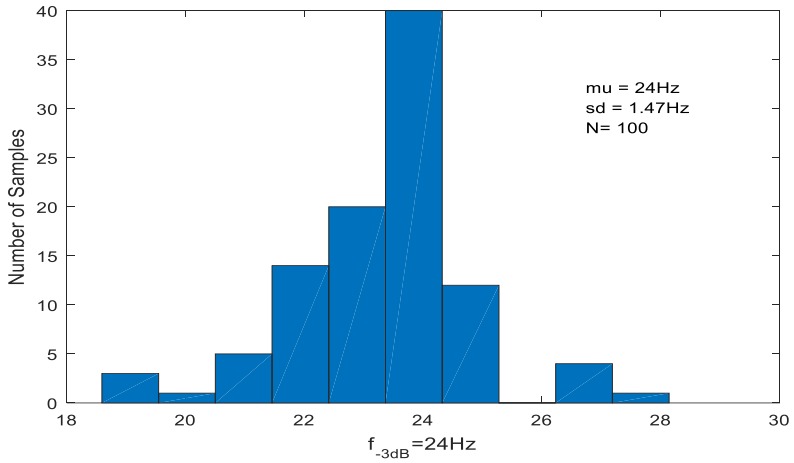


Figure 13. Monte Carlo analysis for $f_{-3dB} = 24$Hz.

Table 3. Comparison between conventional designs and the proposed work.

Parameters	[5]	[16]	[41]	[42]	[43]	[44]	[45]	**This Work**
V_{DD}, V	1	1.8	1.8	1	3	±0.8	0.9	±0.3
Technology, µm	0.18	0.18	0.18	0.18	0.35	0.25	0.13	0.18
Power, µW	0.35	0.57	200	0.453	0.75	30	2.8	0.9nW
DC gain, dB	-8	0	-6	-9.5	-6	-5	5.9	0
Filter order	5	4	5	5	4	5	4	2
THD, dB	-49.9	-40	-44	-48.6	-59	-40	-40	-43

Dynamic range, dB	49.8	56.06	52	50	54	65	43.22	78.2
Bandwidth, Hz	50	50	250	250	40	253	52	50
IRN, μV_{rms}	97	109	266	340	500	36	24.4	9.09
FoM	**0.226**	**0.224**	**100**	**0.286**	**0.374**	**3.3**	**4.83**	**0.00575**

5. Conclusions

In this work, a new implementation for low-pass filter of biomedical data acquisition system developed with DTMOS technique is proposed. The active RC filter is designed with OTA based capacitor multiplier. The cascaded cell-based implementation is performed with the design of capacitor multiplier, which is very appropriate for the low power and low frequency applications where high multiplication factor is required. The proposed structure works with a supply voltage of ± 0.3V and dissipates 0.98nW, whilst the occupation area of core circuit on chip is 0.0083mm^2. The input referred noise of the designed filter is presented around 9.09µV/sqrt(Hz). All simulations are performed in Cadence environment with 0.18µm TSMC technology.

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Authors' contributions

First Author performs the mathematical calculations. Second author simulates the circuit in Cadence environment.
Both authors read and approved the final manuscript.

Competing interests

The authors declare that they have no competing interests.

Ethics in Publishing

There are no ethical issues regarding the publication of this study.

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