# PAPER DETAILS

TITLE: Electrical conduction mechanisms in plasma-enhanced chemical vapor deposited SiO2

dielectric films

AUTHORS: Halit ALTUNTAS

PAGES: 281-287

ORIGINAL PDF URL: https://dergipark.org.tr/tr/download/article-file/342791

GU J Sci 30(3): 281-287 (2017)

Gazi University



**Journal of Science** 



http://dergipark.gov.tr/gujs

# Electrical conduction mechanisms in plasma-enhanced chemical vapor deposited SiO<sub>2</sub> dielectric films

H. ALTUNTAS<sup>1,\*</sup>, S. OZCELIK<sup>2,3</sup>

<sup>1</sup>Department of Physics, Faculty of Science, Cankiri Karatekin University, 18100 Cankiri, TURKEY

<sup>2</sup>Department of Physics, Faculty of Science, Gazi University, 06500 Ankara, TURKEY

<sup>3</sup>Photonics Application and Research Centre, Gazi University, 06500 Ankara, TURKEY

#### Article Info

#### Abstract

Received: 13/03/2017 Accepted: 24/07/2017

# Keywords

PECVD, SiO2, Frenkel-Poole emission, Dielectric

# **1. INTRODUCTION**

In this study, SiO<sub>2</sub> films with thicknesses 50 nm were grown on *n*-GaAs substrate by plasma enhanced chemical vapor deposition technique. To investigate the electrical transport mechanisms, Au/SiO<sub>2</sub>/*n*-GaAs (MOS) type capacitor structures were fabricated and measured current density-voltage (*J*-*V*) characteristics at room temperature. As a function of the applied gate voltage, Schottky emission, Frenkel-Poole emission, and trap-assisted tunneling were found as dominant current transport mechanisms under depletion mode. The obtained trap levels were attributed to defects related with the Ga vacancies formed at the SiO<sub>2</sub>/GaAs interface. *PACS*: 73.30.+y: 73.40.Qv: 73.40.Ns

Silicon dioxide  $(SiO_2)$  is a dielectric material and it has played an important role in the development and evolution of microelectronics industry due to its large band gap (~ 9 eV), high melting temperature, and high resistivity [1-8]. Also SiO<sub>2</sub> has been used as an interfacial layer between high-k dielectric materials and substrates [9-14]. On the other hand, gallium arsenide (GaAs) material is one of the III-V semiconductor compounds and due to its superior electron transport properties compared to silicon, much attention has been focused on GaAs based oxide structures such as SiO<sub>2</sub>/GaAs. In order to achieve good electronic devices, high-electrically quality SiO2 dielectric films should be achieved, which is very closely related to deposition techniques [15-20].

In the present work, SiO<sub>2</sub> dielectric films were deposited on GaAs by plasma enhanced chemical vapor deposition technique (PECVD). Chemical vapor deposition (CVD) is a multifaceted procedure which is currently used for deposition of metals, composites of nonmetallic materials such as carbon, silicon, carbides, nitrides, oxides, and intermetallics. In the CVD technique, a precursor gas (source gas) flows into a chamber, over the heated substrates to be coated, and deposition of thin films on the surface occurs due to the chemical reaction in vapor phase. On the other hand, PECVD is a hybrid technique which uses electrical energy for producing a plasma, and the produced plasma activates the reaction by transferring the energy of its species to the precursors and induces free radical formation. This technique is one of the lowtemperature deposition methods and the advantage of this technique is to deposit silicon oxide with a high deposition rate and at low temperature, that is compatible with a large range of microelectronicoptoelectronic applications [21,22]. Au/SiO<sub>2</sub>/n-GaAs MOS capacitor devices were fabricated and current conduction mechanisms causes the leakage current in the devices were investigated at room temperature. Leakage current causes the instability and loss of power in the electronic circuits. The knowledge of the conduction process in the dielectric films and the discovery of the mechanisms that lead to the leakage current are vital important. For this reason, current-voltage (I-V) measurements of the Au/SiO<sub>2</sub>/n-GaAs MOS capacitors were performed to extract basic electrical parameters and leakage current conduction mechanisms. In our previous study [23], the leakage current mechanisms in thin (3 nm) SiO<sub>2</sub> films were analyzed and Frenkel-Poole emission, ohmic conduction, and space-charge limited conduction mechanisms were found. But in this study, thick  $SiO_2$  (50 nm) films were deposited and found different electrical transport mechanisms.

# 2. EXPERIMENTAL METHOD

The GaAs substrates were n-type, with (100)-orientated wafers and having a thickness of about 350  $\mu$ m. The wafers were dipped into ammonium peroxide for a few seconds to remove native oxide layer on the wafer surface. Au/Ge/Ni alloy was evaporated on the back side of the cleaned GaAs substrate and annealed at 430 oC for 40 seconds to perform ohmic contacts. Insulator layer (SiO<sub>2</sub>) with a thickness of approximately 50 nm was deposited on the upper surface of the GaAs by using plasma enhanced chemical vapor deposition (PECVD) technique. In PECVD system SiH4 gas and O2 gas were used for Si and oxygen sources, respectively. After deposition the dielectric films, the gold film (thickness ~ 100 nm) was subsequently deposited, using an thermal evaporation source onto the surface of the SiO<sub>2</sub> through holes (1 mm diameter) in the metal mask and current density-voltage (J-V) and capacitance-voltage (C-V) measurements were performed to investigate electrical transport mechanisms.

# **3. RESULTS AND DISCUSSION**

The J-V characteristics of the Au/SiO<sub>2</sub>/n-GaAs MOS capacitor devices are given in Fig. 1. As can be seen in fig. 1, current density depends on the applied gate voltage and increases with increasing gate voltage. In ideal case, SiO<sub>2</sub> dielectric films are nearly insulator in which no appreciable leakage current must occur [24]. But, due to insulators are typical dielectric materials, depending on the magnitude of the applied gate voltage, electrical conduction occurs in the dielectric films. In general, these conduction mechanisms were divided into two categories; electrode-limited (conduction occurs due to the electrode/dielectric interface) and bulk-limited (conduction occurs via dielectric defects) conduction mechanisms [24, 25]. In this study, several electrical conduction models were tested to explain the measured J-V curves.



Figure 1. J-V characteristics of the Au/SiO<sub>2</sub>/n-GaAs capacitor devices

Under depletion mode, at low electric fields, the Schottky emission (SE) mechanism is described as

$$J \propto A^* T^2 exp\left[\frac{-q(\phi_B - \sqrt{qE/4\pi\varepsilon_r\varepsilon_o})}{k_B T}\right]$$
(1)

where J, E, A<sup>\*</sup>,  $\phi$ B,  $\epsilon$ r, q, and k are the current density, the electric field, the effective Richardson constant, the barrier height, the dielectric constant of the dielectric films, the electronic charge, and Boltzmann constant, respectively. We point out that having a straight line on the ln (J) versus E1/2 plot does not guarantee SE based conduction. Therefore, it is important to ensure that the obtained dynamic dielectric

constant from the slope of the ln (J) versus E1/2 plot is comparable with static and optical dielectric constants.

Using Eq. (1),  $\epsilon r$  can be calculated from the ln J vs. E1/2 plot (Fig. 2) if SE applies. From the ln J vs. E1/2 graph,  $\phi B$  and  $\epsilon r$  were calculated as 0.63 eV and 3.36, respectively. This dielectric constant value coincides with the static dielectric constant 3.38, which was obtained from the high frequency (at 1 MHz) Capacitance-Voltage (C-V) measurements as shown in fig.3. The dielectric constant ( $\epsilon r$ ) can be calculated on the basis of the formula as C= $\epsilon r \epsilon o A/d$ , where, ; C is the capacitance of the films in strong accumulation, A; area of the capacitor (0,00785 cm2), d; thickness of SiO<sub>2</sub> film (50 nm), and  $\epsilon o$ ; permittivity of free space. Thus, we can safely say that the current conduction mechanism in Au/SiO2/n-GaAs capacitor at low electric fields is due to Schottky emission mechanism. Schottky emission is an electrode-limited conduction mechanism and if the electrons can obtain enough energy provided by thermal activation, the electrons in the metal will overcome the energy barrier at the metal/dielectric interface to go to the dielectric [24].



Figure 2. Schottky emission model fitted for the Au/SiO<sub>2</sub>/n-GaAs capacitor devices.



Figure 3. High frequency (1 MHz) C-V measurements of Au/SiO<sub>2</sub>/n-GaAs capacitor devices.

At medium electric fields, Frenkel-Poole emission (FP) which is a field assisted thermal de-trapping of a carrier from the bulk dielectric material into conduction band can cause the leakage current. Therefore, it is a bulk-limited conduction process. In this mechanism, FP emission can be given as

$$J \propto Eexp\left[\frac{-q(\phi_t - \sqrt{qE/\pi\varepsilon_r\varepsilon_o})}{k_BT}\right]$$
(2)

where  $\phi_t$  is the electrical active trap level within the band gap of the SiO<sub>2</sub>. Ln *J/E* vs.  $E^{1/2}$  plot is given in fig. 4, and according to Eq. (2), the slope of fig. 4 provides an estimate of the dielectric constant of SiO<sub>2</sub> dielectric film. As can be seen in fig. 4, the plot is very well fitted (R<sup>2</sup> = 0.999) with the FP mechanism, and  $\phi_t$  and  $\varepsilon_r$  were calculated to be 0.45 eV and 3.92, respectively.



Figure 4. Frenkel-Poole plot of the Au/SiO2/n-GaAs capacitor structures

The calculated dielectric constant value was in good agreement with the static dielectric constants (3.38) and it can be said that the current conduction at medium electric field is due to FP-emission mechanism. The obtained energy level of the electrically active defect states was found as 0.45 eV and this value is coincides with the value reported by Deenapanray [26] and Burkner [27]. They have explained these trap levels with 0.45 eV as excess gallium vacancies ( $V_{Ga}$ ) defects generated at the SiO<sub>2</sub> /GaAs interface by the migration of gallium atoms into the SiO<sub>2</sub> dielectric films. Therefore, the obtained traps levels at medium electric fields were attributed to Ga atoms in the SiO<sub>2</sub> dielectric films and they cause FP-emission from the dielectric layer into the conduction band of semiconductor.

Finally, at higher electric fields, the current density was fitted by the trap assisted tunneling (TAT). The current due to TAT mechanism is given by

$$J_{TAT} \propto exp\left\{\frac{-8\pi\sqrt{2qm_{AIN}}}{_{3hE}}\phi_t^{3/2}\right\}$$
(3)

where  $\phi_t$  is energy level of the electronic defects in the band gap of the dielectric. Using the Eq. (3),  $\phi_t$  was obtained from Fig. 5 as 0.47 eV.



Figure 5. TAT- plot of the Au/SiO<sub>2</sub>/n-GaAs capacitor structures.

The obtained  $\phi_t$  value is very close to 0.45 eV that predicted for V<sub>Ga</sub> defects generated at the SiO<sub>2</sub> /GaAs interface. In general, the leakage current via tunneling decreases as an exponent function with increasing film thicknesses. But even in a thicker gate dielectric, if the high amount of the traps localized in the dielectric film or at the interface between the dielectric and semiconductor, these traps play an active role in the formation of the leakage current at higher gate electric field. Some studies have been reported related with the current conduction in SiO<sub>2</sub> films. For example, Lim et al. [28] reported that Schottky emission and Frenkel-Poole emission were found as dominant mechanisms in atomic layer deposited SiO2 films at low and high electric field, respectively. In addition, they have stated that the film thickness is one the key parameter which influences on the electrical conduction mechanisms. Ravindra et al. [29] reported that Fowler-Nordheim tunneling was dominant conduction mechanism in SiO<sub>2</sub> films. Perera et al. [30] reported that ohmic conduction, trap-assisted tunneling, and Fowler-Nordheim tunneling was basic conduction mechanisms in nitrided SiO<sub>2</sub> films.

### 4. CONCLUSION

In this work, SiO<sub>2</sub> dielectric films were deposited on *n*-GaAs substrates by the PECVD technique. Current transport mechanisms of the fabricated Au/SiO<sub>2</sub>/*n*-GaAs capacitor structures were investigated over a wide range of applied electric fields under depletion mode. Depending on the applied electric fields, current conduction mechanisms were found as Schottky emission, Frenkel-Poole emission, and trap assisted tunneling. The calculated energy levels of the electronic defects are attributed to the excess vacancies ( $V_{Ga}$ ) generated at the SiO<sub>2</sub>/GaAs interface by the out-diffusion of Ga atoms into the SiO<sub>2</sub> dielectric films.

#### ACKNOWLEDGMENTS

The Authors would like to thank Michael Schneiderman at Submicron Research Center at Weizmann Institute of Science for SiO<sub>2</sub> coating by PECVD. This study was supported by the Turkish Prime Ministry state Planning Agency under project no: 2001K120590 and The European Transnational Access Program # RITA-CT-2003-506095 WISSMC.

#### **CONFLICT OF INTEREST**

No conflict of interest was declared by the authors

## REFERENCES

- [1] Sze, S. M., Physics of Semiconductor Devices, 2nd ed., Wiley, New York, (1981).
- [2] Choi, H., Kim, T. G., Shin, C., "Measurement of the quantum capacitance from two-dimensional surface state of a topological insulator at room temperature", Applied Surface Science, 407: 16-20, (2017).
- [3] Samoju, V. R., Mohapatra, S., Bhushan, S., Tiwari, P. K., "Analytical Modeling and Simulation of Subthreshold Characteristics of Recessed-Source/Drain (Re-S/D) Silicon-on-Insulator MOSFETs with Gaussian Doping Profile", Journal of Nanoelectronics and Optoelectronics, 12: 490-498, (2017).
- [4] Ma, Y., Gao, B., Gong, M., Willis, M., Yang, Z., Guan, M., Li, Y., "High fluence swift heavy ion structure modification of the SiO<sub>2</sub>/Si interface and gate insulator in 65nm MOSFETs", Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, 396: 56-60, (2017).
- [5] He, X., Sun, Z., Pang, Y., Li, Y., "In-situ detection of local avalanche breakdown and large magnetoresistance in Ag/SiO<sub>2</sub>/p-Si: B/SiO<sub>2</sub>/Ag device", Journal of Applied Physics, 121: 114501, (2017).
- [6] Tsuchiyama, K., Yamane, K., Utsunomiya, S., Sekiguchi, H., Okada, H., Wakahara, A., "Monolithic integration of Si-MOSFET and GaN-LED using Si/SiO<sub>2</sub>/GaN-LED wafer", Applied Physics Express, 9:104101, (2016).
- [7] Liu, M. J., Huang, G. S., Feng, P., Guo, Q. L., Shao, F., Tian, Z. A., Mei, Y. F., "Nanogranular SiO<sub>2</sub> proton gated silicon layer transistor mimicking biological synapses", Applied Physics Letters, 108: 253503, (2016).
- [8] Efthymiou, E., Rutter, P., & Whiteley, P., "A methodology for projecting SiO<sub>2</sub> thick gate oxide reliability on trench power MOSFETs and its application on MOSFETs V GS rating", Microelectronics Reliability, 58: 26-32, (2016).
- [9] Nadimi, E., Planitz, P., Ottking, R., Schreiber, M., Radehaus, C.," Single and Multiple Oxygen Vacancies in Ultrathin SiO<sub>2</sub> Gate Dielectric and Their Influence on the Leakage Current: An Ab Initio Investigation", IEEE Electron Dev. Letters, 31: 881-883, (2010).
- [10] Cao, Y. Q., Wu, B., Wu, D., Li, A. D., "Interfacial, Electrical, and Band Alignment Characteristics of HfO<sub>2</sub>/Ge Stacks with In Situ-Formed SiO<sub>2</sub> Interlayer by Plasma-Enhanced Atomic Layer Deposition", Nanoscale Research Letters, 12:370-7, (2017).
- [11] Manikanthababu, N., Chan, T. K., Vajandar, S., Saikiran, V., Pathak, A. P., Osipowicz, T., Rao, S. V. S. N., "Ion induced intermixing and consequent effects on the leakage currents in HfO<sub>2</sub>/SiO<sub>2</sub>/Si systems", Applied Physics A-Materials Science & Processing, 123: 303-7, (2017).
- [12] Sharma, A., Varshney, M., Kang, S., Baik, J., Ha, T. K., Chae, K. H., Kumar, S., Shin, H. J.," Electronic structure study and dielectric properties of amorphous ZrO<sub>2</sub> and HfO<sub>2</sub>", Adv. Mater. Lett., 7: 17-22, (2016).
- [13] Park, I. S., Lee, T., Ko, H., Ahn, J., "Electrical and reliability characteristics of HfO<sub>2</sub> MOS capacitor with Mo metal gate electrode", Journal of the Korean Physical Society, 49: S760-S763, (2016).
- [14] Hung, C. H., Wang, S. J., Liu, P. Y., Wu, C. H., Wu, N. S., Yan, H. P., & Lin, T. H., "A room temperature process for the fabrication of amorphous indium gallium zinc oxide thin-film transistors with co-sputtered Zr<sub>x</sub>Si<sub>1-x</sub>O<sub>2</sub> Gate dielectric and improved electrical and hysteresis performance", Japanese Journal of Applied Physics, 56: 04CG06, (2017).
- [15] Kochowski, S., Nitsch, K., "Description Of The Frequency Behaviour Of Metal–SiO<sub>2</sub>–GaAs Structure Characteristics By Electrical Equivalent Circuit With Constant Phase Element", Thin Solid Films, 415: 133-137, (2002).

- [16] Mochizuki, Y., Mizuta, M., "Initial Oxidation Of Si (100)-(2 × 1)H Monohydride Surfaces Studied By Scanning Tunneling Microscopy/Scanning Tunneling Spectroscopy", Appl. Surf. Sci., 117: 114-118 (1997).
- [17] Eftekhari, G., "The Electrical Properties Of Sulfur-Passivated And Rapidly Thermally Annealed GaAs Metal-Oxide-Semiconductor Structures With The Oxide Layer Grown Anodically", Thin Solid Films, 248: 199-203, (1994).
- [18] Lefebvre, P. R., Lai, L., Irene, E. A., "Comparison Of The Structure And Electrical Properties Of Thermal And Plasma Grown Oxides On GaAs", J. Vac. Sci. Technol. B, 16: 996-1001 (1998).
- [19] Gaman, V. I., Kalygina, V. M., Panin, A. V., "Effect Of Chalcogenide Elements On The Electrical Characteristics Of GaAs MIS Structures", Solid State Electron., 43: 583-588, (1999).
- [20] Balakrishnan, V. R., Kumar, V., Ghosh, S., "Conductance Deep-Level Transient Spectroscopic Study Of Anomalous Hole Trap In GaAs Mesfets", Semicond. Sci. Technol., 13: 1094-1099, (1998).
- [21] Viana, C. E., Da Silva, A. N., Morimoto, N. I., Bonnaud, O., "Analysis of SiO2 thin films deposited by PECVD using an oxygen-TEOS-argon mixture", Brazilian Journal of Physics, 31: 299-303, (2001).
- [22] Hamedani, Y., Macha, P., Bunning, T. J., Naik, R. R., Vasudev, M. C., "Plasma-Enhanced Chemical Vapor Deposition: Where we are and the Outlook for the Future", Chemical Vapor Deposition-Recent Advances and Applications in Optical, Solar Cells and Solid State Devices, Chapter (10), InTech, (2016).
- [23] Altuntas, H., Ozcelik, S., "The Analysis of Leakage Current in MIS Au/SiO<sub>2</sub>/*n*-GaAs at Room Temperature", Semiconductors, 47: 1308-1311, (2013).
- [24] Chiu, F. C., "A Review On Conduction Mechanisms In Dielectric Films", Adv. Mat. Sci. Eng., 578168-18, (2014).
- [25] Simmons, J. G., Electronic conduction through thin insulating films," in *Handbook of Thin Film Technology*, L. Maissel and R. Glang, Eds., chapter 14, McGraw-Hill, New York, NY, USA, (1970).
- [26] Deenapanray, P. N. K., Tan, H. H., Jagadish, C., "Investigation Of Deep Levels In Rapid Thermally Annealed SiO<sub>2</sub>-Capped N-GaAs-GaAs Grown By Metal-Organic Chemical Vapor Deposition", Appl. Phys. Lett., 77: 696-698, (2000).
- [27] Burkner, S., Maier, M., Larkins, E. C., Rothermound, W., O'Reilly, E. P., Ralston, J. D., "Process Parameter Dependence Of Impurity-Free Interdiffusion In GaAs/Al<sub>x</sub>Ga<sub>1-x</sub>As And In<sub>x</sub>Ga<sub>1-y</sub>As/GaAs Multiple Quantum Wells", J. Electron. Mater., 24: 805-812 (1995).
- [28] Lim, J. W., Yun, S. J., & Lee, J. H., "Low-temperature growth of SiO2 films by plasma-enhanced atomic layer deposition", ETRI Journal, 27: 118-121, (2005).
- [29] Ravindra, N. M., Zhao, J., "Fowler-Nordheim tunneling in thin SiO<sub>2</sub> films", Smart Materials and Structures, 1: 197-201, (1992).
- [30] Perera, R., Ikeda, A., Hattori, R., Kuroki, Y., "Trap assisted leakage current conduction in thin silicon oxynitride films grown by rapid thermal oxidation combined microwave excited plasma nitridation", Microelectronic Engineering, 65: 357-370, (2003).