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Interface Effects of Annealing Temperatures in Al/HfO₂/p-Si (MIS) Structures

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Abstract

In this study, Al/HfO₂/p-Si (MIS) structures were prepared by using the sol-gel method for three different annealing temperatures. The current-voltage (I-V) and capacitance-voltage (C-V) characteristics of these structures were investigated by taking into consideration the effect of the interfacial insulator layer and surface states (N_{ss}) at room temperature. All of the structures showed non-ideal I-V behaviour with ideality factor (n) in the range between 2.35 and 4.42 owing to interfacial insulator layer and surface states. The values of N_{ss} and barrier height (ϕ_b) for three samples were calculated. The values of n and N_{ss} ascend with increasing the insulator layer thickness (δ) while the values of ϕ_b decreases.

1. INTRODUCTION

Metal-semiconductor (MS) and metal-oxide-semiconductor (MOS) diodes are of great importance for contributing to the understanding of the semiconductor surface and surface states. Any insulator layer, produced between metal and semiconductor by means of the natural or deposition process, causes the metal-insulator-semiconductor (MIS) diode having non-ideal behavior. Thus, the “ideality factor (n), surface states (N_{ss}), and barrier height (ϕ_b) of an MIS structure significantly differ from the expected magnitudes, which is mainly caused by the potential drop across the insulate layer due to the interface states at insulator/Si interface [1-7]. Recently, the growth of various insulators on single crystalline silicon, such as SnO₂ [8], Si₃N₄ [9], TiO₂ and hafnium dioxide (HfO₂) [10-11], in MIS structures has been subject to extensive research as an alternative to silicon-dioxide (SiO₂). The small number of surface states, high dielectric permittivity and high breakdown voltage are among the important advantages of these films when compared to SiO₂. MIS diodes produced by HfO₂ thin films are also of considerable importance due to the same advantages.

HfO₂ is one of the most common and stable compounds of hafnium. Therefore HfO₂ is used in optical coatings, and as a high- κ dielectric in DRAM capacitors and in advanced metal-oxide-semiconductor devices [12]. In view of the these facts, the experimental investigations on Al/HfO₂/p-Si (MIS) structures prepared by the sol-gel method at three different preparation temperatures have been carried out and their main electrical parameters such as ϕ_b , n and N_{ss} have been investigated by taking into account the effect of the interfacial insulator layer. To explain the forward bias I-V and C⁻²-V characteristics, the model provided in literature has been used [3-6].

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2. EXPERIMENTAL

2.1. Al/HfO₂/p-Si Structures Preparation

To prepare the HfO₂ solution, 0.0063 mol hafnium tetrachloride was dissolved in 15 mL ethanol, to which 0.08 mol H₂O and 0.013 mol HNO₃ were added and the solution was kept in a magnetic stirrer for 2 hours. Finally, before coating the film, the solution was maintained at 50 °C for 4 hours.

Metal-oxide-semiconductor (Al/HfO₂/p-Si) structures were manufactured on the 1-inch diameter float zone (100) p-type (boron-doped) single crystal silicon wafer with a thickness of 280 µm and a resistivity of 1–10 Ω.cm. For the fabrication process, Si wafer was degreased through the RCA cleaning process (i.e., a 10 minute boiling in NH₄OH + H₂O₂ + 6 DI (18 MΩ deionised water), which was followed by a 10 minute boiling in HCl + H₂O₂ + 6 DI [10, 13]. Then, it was subjected to the drying process in N₂ atmosphere for a duration time. After that, high-purity aluminum with a thickness of 1500 Å was thermally evaporated from the tungsten filament onto the whole back surface of the Si wafer under the pressure of 10⁻⁶ Torr. In order to obtain a low-resistivity ohmic back contact, Si wafer was sintered at 580 °C for 3 minutes in N₂ atmosphere. The native oxide on the front surface of the substrate was removed in HF : H₂O (1 : 10) solution, and finally, the wafer was rinsed in deionised water for 30 s before forming an HfO₂ layer on the p-type Si substrate. The prepared HfO₂ solution was coated on the shiny side of the cleaned p-Si surface at 2000 rpm by the sol-gel spinning technique. The HfO₂/p-Si structures were annealed for five minutes at 100, 200, and 300 °C in N₂ atmosphere after each coating process. The process was repeated in the same way until the required film thickness was obtained and the structure was finally exposed to annealing at 500 °C in N₂ atmosphere for 1 h.

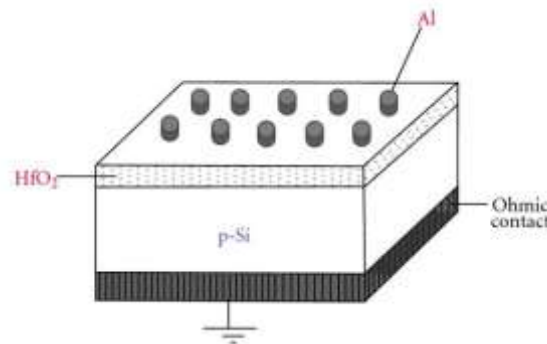


Figure 1. Schematic diagram of Al/HfO₂/p-Si (MIS) structure.

A high-purity aluminum layer (2000 Å) was coated on the surface in a vacuum under the pressure of 10⁻⁶ Torr in order to obtain a rectifying contact on the front surface of p-Si coated with HfO₂. The structure of Al/HfO₂/p-Si/Al (MIS) structures is given in Figure 1. The preparation data of HfO₂ thin films on Si wafer substrate are given in Table 1.

Table 1. Preparation data of HfO₂ thin films prepared on Si wafer substrate.

Nr.	Structure	Treatment Temperature and Time	Insulator layer, thickness δ(Å)
S1	Al/HfO ₂ /p-Si	100 °C, 5 min.	126
S2	Al/HfO ₂ /p-Si	200 °C, 5 min.	108
S3	Al/HfO ₂ /p-Si	300 °C, 5 min.	95

2.2. Characterization

The insulator layer thicknesses of prepared devices were measured by Avantes spectrometer (AvaSpec-ULS2048). The current-voltage (I - V) and capacitance-voltage (C - V) measurements, carried at 500 kHz with a test signal of 50 mV_{rms}, were performed by Keithley-4200 semiconductor characterization system (SCS) at room temperature and in a darkened and sealed metal box, respectively.

3. RESULTS AND DISCUSSION

The energy band diagram of an MIS structure at forward bias is presented in Figure 2. The parameters ϕ_m , χ , Δ and δ are the work function of metal, the electronic affinity of the semiconductor, the voltage drop across the interface insulator layer, and the thickness of the insulator layer, respectively. The parameter ϕ_0 is commonly defined as the neutral level of surface states taken from the valance band edge at the semiconductor surface [14]. V_p is the potential difference between the Fermi level and the top of valance band in the neutral region, and ϕ_e is the effective barrier height.

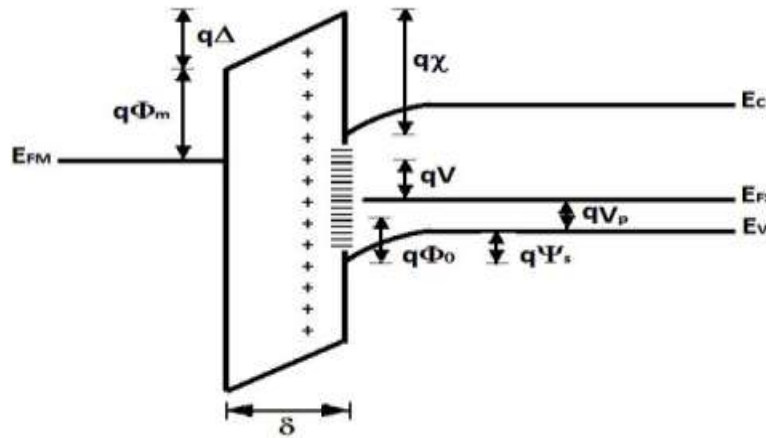


Figure 2. The energy band diagram of a MIS system under non-equilibrium condition.

From the energy band diagram, the potential drop Δ across the interface layer can be determined by Gauss's law [7, 14];

$$\Delta = -\left[\frac{E_g}{q} + \chi - \phi_e - \phi_m \right] = \frac{\delta}{\epsilon_i} (Q_{sc} + Q_{it} + Q_f) \quad (1)$$

where Q_{sc} is the semiconductor depletion layer charge, Q_{it} is the interface trap charge at bias V , Q_f is the fixed surface charge at the semiconductor interface and ϵ_i is permittivity of the insulator layer. The depletion charge is given by

$$Q_{sc} = -[2q\epsilon_s N_A (\phi_e - V_n)]^{1/2} \quad (2)$$

where N_A is the doping concentration and ϵ_s is the permittivity of semiconductor. The interface state charge is:

$$Q_{it} = -qN_{ss} (q\phi_e - q\phi_0) \quad (3)$$

where N_{ss} is the density of the interface states. From the above equations, the following expressions can be written as:

$$c_1 = 2q\epsilon_s N_A \delta^2 / \epsilon_i^2 \quad (4a)$$

$$c_2 = \epsilon_i / (\epsilon_i + q^2 \delta N_{ss}) \quad (4b)$$

$$\phi_e = c_2 (E_g / q + \chi - \phi_m) + (1 - c_2) \phi_0 + c_2 (\delta Q_f / \epsilon_i) = \phi_b + c_2 (\delta Q_f / \epsilon_i) \quad (4c)$$

where ϕ_b is the barrier height without fixed surface charge at thermal equilibrium and can be defined by

$$\phi_b = c_2 (E_g / q + \chi - \phi_m) + (1 - c_2) \phi_0 \quad (5)$$

The depletion layer capacitance per unit area of a MS contact without interfacial layer can be given by

$$C = [q\epsilon_s N_A / 2(V_d - V)]^{1/2} \quad (6)$$

From equation (6), the quantity of C^{-2} can be written as

$$C^{-2} = 2(V_d - V) / q\epsilon_s N_A \quad (7)$$

When a metal-semiconductor contact with interfacial layer (MIS) is considered, the depletion capacitance C can be become [2],

$$C = c_2 \left\{ q\epsilon_s N_A / 2 [\phi_b - c_2 V - V_n + c_2 (\delta Q_f / \epsilon_i)] \right\}^{1/2} \quad (8)$$

and

$$C^{-2} = 2 [\phi_b - c_2 V - V_n + c_2 (\delta Q_f / \epsilon_i)] / c_2^2 q\epsilon_s N_A \quad (9)$$

c_2 can be written as follows from the slope of the C^{-2} - V plot

$$c_2 = \frac{2}{q\epsilon_s N_A \left[d(C^{-2}) / dV \right]} \approx \frac{N'_A}{N_A} \quad (10)$$

where N'_A is the experimental value of doping concentration and N_A is the theoretical value of doping concentration. From the intercept of C^{-2} - V plot with the voltage axis, the value of ϕ_b can be obtained as

$$\phi_b = (c_2 V_0 + V_n) - c_2 (\delta Q_f / \epsilon_i) \quad (11)$$

From equations (6) and (11), the effective barrier height at thermal equilibrium may be defined as

$$\phi_e = (c_2 V_0 + V_n) \quad (12)$$

where V_0 is the intercept voltage. According to equation (11), the barrier height without the fixed surface charge can be given by

$$\phi_b = (c_2 V_0 + V_n) \quad (13)$$

In order to obtain ϕ_b or ϕ_e , from equations (12) and (13), it is necessary to know the Fermi energy V_n . From equation (4b), the value of c_2 is a function of δ and N_{ss} .

Capacitance-voltage (C - V) measurements are performed at a sufficiently high frequency ($f \geq 500$ kHz) to prevent the interface states responding to the ac signal [15, 16]. Therefore, the forward and reverse bias C - V characteristics at 500 kHz for three different annealing temperatures are shown in Figure 3. The applied voltage was varied between -4 V and +4 V. From an MS or MIS structure, the doping density concentration (N_A), and the diffusion potential (V_d) can be directly achieved from the slope and the intercept with the voltage axis of C^{-2} vs. V plot [1, 2]. C^{-2} vs. V plots were shown in Figure 4. Values of N_A and c_2 were calculated for all structures according to Eq. (10) using the slope data obtained from C^{-2} vs. V plots.

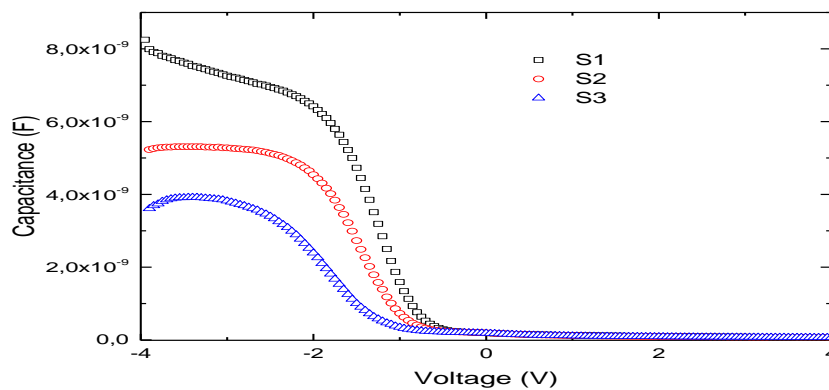


Figure 3. High frequency (500kHz) capacitance – voltage characteristics of Al/HfO₂/pSi (MIS) structures at room temperature.

Then the values of ϕ_b were calculated, as the values of c_2 and V_n are known. There is a linear correlation between ϕ_b and c_2 as shown in Figure 5. From the extrapolation of the line to $c_2=1$ the value of ϕ_b was found to be equal to 1.032 eV and also from the extrapolation of that to $c_2=0$ the value of neutral level ϕ_0 of surface states was obtained as 0.12 eV.

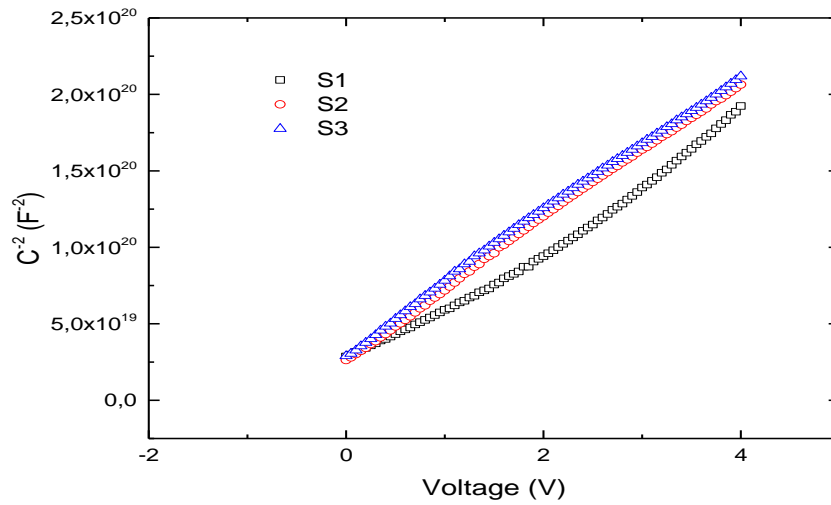


Figure 4. C^2 - V characteristics for 500 kHz of the Al/HfO₂/p-Si MIS structures at room temperature.

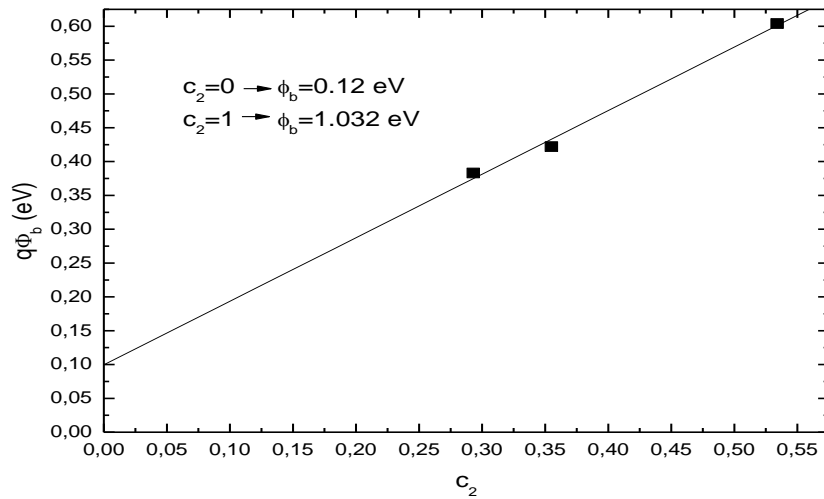


Figure 5. ϕ_b - c_2 plot of the Al/HfO₂/p-Si MIS structures at room temperature.

Due to the existence of an insulator layer at M/S interface, it is assumed that there is a relation between the applied forward bias voltage V ($V > 3kT/q$) and the current I . According to the thermionic emission (TE) theory, the current is expressed as [1],

$$I = I_0 \exp \left[\frac{qV}{(1 + q^2 \delta N_{ss} / \epsilon_i) kT} \right] \quad (14)$$

where I_0 is the reverse saturation current and is given as

$$I_0 = AA^* T^2 \exp \left(- \frac{q\phi_b}{kT} \right) \quad (15)$$

where ϕ_b , A , A^* , n , q and T are zero-bias barrier height, the rectifier contact area, the effective Richardson constant ($32 \text{ A/cm}^2 \text{ K}^2$ for p-type Si), ideality factor, the electron charge and the temperature in K, respectively. The value of $1 + q^2 \delta N_{ss} / \epsilon_i$ can be considered as the ideality factor of the MIS structure. According to equation (4b), this factor should be equal to $1/c_2$.

Figure 6 shows the forward bias $\ln I$ - V characteristics of Al/HfO₂/p-Si (MIS) structures at the room temperature. The determined values of the ideality factor (n) range from 2.35 to 4.42. These values of n are appreciably high. Such behavior of ideality factor can be attributed to the interfacial insulator layer and interface states.

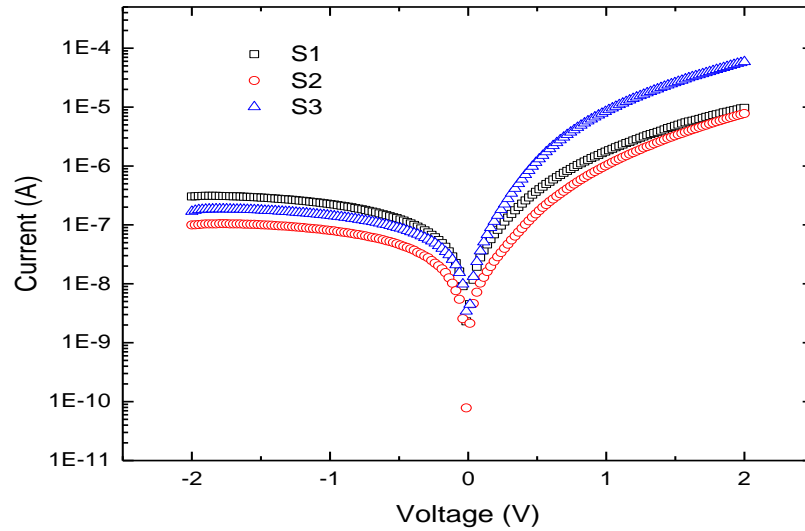


Figure 6. $\ln I$ - V characteristics of Al/HfO₂/p-Si (MIS) structures at room temperature.

For a sufficiently thick interfacial insulator layer, the interface states are in equilibrium with the semiconductor and they cannot interact with the metal [2, 7, 14]. When N_{ss} are in equilibrium in semiconductor, the general expression for the ideality factor, as deduced by Chard and Rhoderick [2], reduces to

$$n = 1 + \frac{\delta}{\varepsilon_i} \left[\frac{\varepsilon_s}{W_D} + qN_{ss} \right] \quad (17)$$

where W_D is the width of the depletion region and expressed as

$$W_D = \left[(2\varepsilon_s / qN_A) V_d \right]^{1/2} \quad (18)$$

Substituting the value of permittivity of HfO₂ ($\varepsilon_i = 25\varepsilon_0$) [17, 18] and the thickness of δ in equations (17), the value of density of N_{ss} for three different repeated annealing temperatures were thus obtained. In addition, the values of density of N_{ss} for three different annealing temperatures were also obtained by using the value of c_2 and δ in equation (4b). These results were given in Table 2. As can be seen in Table 2, in these two cases, the value of density of interface states increases with increasing insulator layer thickness.

Table 2. Various parameters obtained from C - V (500 kHz) and I - V characteristics of Al/HfO₂/p-Si (MIS) structures at room temperature.

Nr.	$1/c_2$	n	ϕ_b (C-V) (eV)	N_{ss} ($1/c_2$) (10^{13} eV ⁻¹ cm ⁻²)	N_{ss} (n) (10^{13} eV ⁻¹ cm ⁻²)
S1	4.92	4.42	0.434	2.303	2.132
S2	3.81	3.21	0.574	2.054	2.258
S3	2.54	2.35	0.638	1.357	1.654

There is a difference between obtained barrier heights from C-V and I-V measurements. This situation frequently reported for MIS and MOS devices and can be caused by the existence of an interfacial layer and barrier inhomogenities. Sensitivities of C-V and I-V techniques to these effects are different [19].

4. CONCLUSION

The *I-V* and *C-V* characteristics of Al/HfO₂/p-Si (MIS) structures by using the sol-gel method were measured at room temperature for three different annealing temperatures. The calculated values of *n* were found in the range between 2.35 and 4.42, which may be the cause of the interface states densities localized at HfO₂/p-Si interface and the effect of insulator layer thicknesses at Al/p-Si interface. The values of *N_{ss}* for three samples with different insulator layer thickness were also calculated. While the values of *n* and *N_{ss}* decrease with decreasing the insulator layer thickness, the values of ϕ_b increase. In addition, the value of ϕ_b and ϕ_0 was obtained to be 1.032 eV and 0.12 eV with help of correlation between ϕ_b and *c₂*, respectively. The experimental results caused by the thickness-dependent change in the interface states of insulator layers were consistent with the previous studies [3, 7]. Moreover, the obtained values of interface states were comparable with the order of magnitude of Al/SnO₂/p-Si and Al/SiO₂/p-Si (MIS) structures [20, 21].

CONFLICT OF INTEREST

No conflict of interest was declared by the authors

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